Technical Guidance

The intent of the Microelectronics Commons is to establish a network of regional hubs to evolve laboratory prototypes to fabrication prototypes (lab-to-fab). In particular, innovative prototype demonstrations in microelectronics materials, processes, devices, and architectural designs will be supported. Peripheral activities pursued as stand-alone topics are not within scope of the Commons hubs unless they are essential for lab-to-fab demonstration of the prototype.

Activities executed within Microelectronics Commons shall primarily fall under Budget Activity 3. Although activities that fall under Budget Activities 2 and 4 will also be supported if they are in support of the lab-to-fab prototype. For further discussion on research, development, testing and evaluation (RDT&E) budget activities, see https://comptroller.defense.gov/Portals/45/documents/fmr/archive/02barch/02b_05old.pdf. For further discussion on Technology Readiness Levels (TRLs) referenced in the Budget Activities document, see https://apps.dtic.mil/sti/pdfs/ADA418881.pdf. For further discussion on Manufacturing Readiness Levels (MRLs), see https://www.dodmrl.com/MRL_Deskbook_V2.pdf.

The Commons will support prototyping capabilities for six technical areas for the DoD. Those areas are: Secure Edge/Internet of Things (IoT) Computing, 5G/6G Technology, Artificial Intelligence Hardware, Quantum Technology, Electronic Warfare, and Commercial Leap Ahead Technologies. The below desired end-state prototype descriptions are provided as technical guidance for the advancements needed in each technical area.

A. Secure Edge/IoT Computing

The desired end-state of secure edge computing is the prototyping of microelectronics technologies based on lab-to fab transition of novel materials, devices and architectures that enable future mission security and assurance. The rapid proliferation of autonomous systems requires more capable computing technologies to drive the performance, assurance, and resilience needed for the contested threat environments of the future. The integration of these elements into national information systems for edge computing will protect the integrity, confidentiality, and availability of our information systems by preventing the loss of control, exfiltration, or manipulation of our Critical Program Information (CPI), deterring adversaries, and providing a means to react in all circumstances.

Secure processing architectures with varying input/output (I/O), processing capabilities, and size, weight, and power (SWaP) plus security (SWaP+S) constraints are required to meet multiple needs of the Defense Industrial Base. The development of a family of holistic secure processing architectures for a wide variety of DoD application spaces is a priority. These application spaces include space, nuclear, air/ground/sea platforms, embedded, attritables, IoT, etc. Secure processing architectures will be designed to utilize state-of-the-art technology that can advance and demonstrate lab-to-fab prototyping, and other fabrication facilities as applicable to air, space, and terrestrial domains. New approaches to edge computing must holistically consider the functionality of the platform.

Secure edge computing platforms generally share a set of desirable characteristics that include hardware assurance. Low SWaP and cost (SWaP+C) devices and certain operating conditions may impose constraints; therefore, necessitating solutions that scale to the resources available, as well as a distributed trust model to generate and share trustworthy data. Proposed architecture must utilize digital engineering best practices such as hardware/software co-development, virtual verification and validation, digital twinning, hardware accurate digital models, future proof designs (no vendor lock), domain specific architectures, differentiated IP access and ownership rights, shared and access-controlled repositories, and modular architectures such that multiple

programs can leverage the same technology.

Properties desirable for secure edge computing include, but are not limited to, 1) advancements in SWaP+S metrics required for future edge computing assets; 2) physical and cyber protection capabilities to provide a holistic security posture to protect the control flow of the processor from external influence, ensure the integrity of the system during execution, prevent exfiltration of information and CPI, and provide a means to recover from threat events; and 3) capabilities to pair secure processors with untrusted high performance computing elements.

It is re-highlighted that peripheral activities pursued as stand-alone topics are not within scope unless they are essential for lab-to-fab demonstration of the prototype. Examples of such peripheral activities may include 1) design for testability and verification, 2) innovations and enhancements in cyber and physical defenses, 3) unique modifications to software and algorithms to take advantage of performance and the security features of the hardware components, and 4) new technologies enabling resiliency in operational environments. Advances being sought include but are not limited to the following:

Family of Secure Processing Architectures for a variety of Edge Computing Application Spaces

The DoD need for secure computing architectures covers a wide range of application spaces. Each application space comes with their unique defining attributes, such as radiation for space, safety for nuclear, SWAP for IoT, etc. Despite their similarities and differences each application space requires a holistic security approach tailored to the need for that space. The DoD seeks a family of advanced holistic secure processing architectures that takes into consideration the varying tradeoffs between SWAP, performance, and security. A holistic security approach incorporates varying degrees cybersecurity, anti-tamper protections, and cryptography, tailored for each target application space. Exemplar efforts include lightweight embedded secure processors for IoT devices, general purpose secure processors for embedded systems, high reliability/safety/assured secure processors for space and nuclear systems, etc.

Secure Computing Approaches

Edge computing requires new approaches to increasing security and limiting SWaP impact on battlefield platforms for fast decision making. Example lab-to-fab microelectronics solutions for this technical area include, but are not limited to, disruptive advances in State-of-the-practice (SoTP)/ State-of-the-art (SoTA) digital fabrication processes that build in security for ADC/DAC, logic, and memory. These advances are necessary as the DoD shifts toward digitizing sensor data with increased processing power.

Packaging for Enhanced Security

Secure edge computing platforms require a holistic security approach to protect CPI residing within the silicon fabric as well as across the heterogeneously integrated (HI) packaged module. Holistic security posture includes cryptographic accelerators, hardware-based cybersecurity, and physical security protection (invasive and non-invasive) applicable to platforms operating both terrestrially and in space. Additionally, this approach not only addresses security within the fabric of the CMOS or ASIC but incorporates inter-chip security (including interfaces (I/O) and interconnects), and package level security, including the ability to detect and respond to invasive and non-invasive attack vectors. As the DoD and commercial sector move toward SoTP/SoTA nodes, advances in HI and advanced packaging (AP) not only increase performance through greater packaging density and mixed signal chiplet integration, but inherently increase the threat surface for an attacker to exfiltrate CPI. Security solutions should be considered as they relate directly to the integration and packaging of multi-chip-modules (MCMs) that are comprised of trusted and untrusted IP and should be extended to chips that are fabricated using SoTP/SoTA HI/AP methods. Solutions should consider 1) securing the IP block, 2) securing the interposer 3) managing chips (trusted vs. untrusted) for inter-chip security, and 4) package level security. The approaches may include passive and/or active sensor(s) for threat detection, and response effects to neutralize the tamper event (response can be kinetic or non-kinetic). These sense and

response methods can be integrated at various levels of the packaging architecture, whether at the die level, die-encapsulant interface, or embedded within the package itself. Packaging and security should be considered complimentary to each other.

B. 5G/6G Technology

The desired end state of Microelectronics Commons 5G/6G is an ecosystem providing integrated, resilient, low-latency connectivity to the battlefield, supporting real-time processing and decision-making. Communication systems must support dismounted and disadvantaged users with both a mixed DOD-purpose built and commercial, resilient, terrestrial, airborne, and space segment, along with low-cost user equipment that can leverage commercial systems. Future Generation (5G/6G) radio frequency (RF) technology advancements are needed for the DoD to connect a wide variety of DoD platforms into secure networks that remain protected from adversaries. Future Generation RF connectivity is predicated on secure, efficient and broadband RF microelectronics technology in the RF, microwave, and millimeter-wave (mmW) bands. As operational complexity increases in the modern electromagnetic spectrum environment, communication systems must a) operate efficiently in tightly congested and potentially narrow frequency channels, b) be flexible over wide bandwidths, c) support spectral agility and sensing, d) offer real-time reconfiguration and autonomous operation when applicable, and e) adaptively handle interference to ensure and optimize datalink and network performance. In addition, such systems must encode and decode, process, and transport vast quantities of data across networks generated by a variety of systems integrated in DoD platforms, by radiofrequency (RF), optical, infra-red, or others.

5G/6G technologies consists of microelectronics solutions addressing 1) high-linearity radio frequency device technology with high power-added efficiency for operation in emerging Future G bands of interest (microwave and mm-wave spectrum) 2) ultra-efficient RF integrated circuit design topologies delivering communications solutions for power dense systems; 3) cognitive and software-defined radios and networks with the ability to tune/reconfigure based on the receiving requirements/needs and latest advancements in autonomous control and hybrid microelectronic architectures 4) secure, low-latency, and high-speed data rate communications chip-sets capable of encoding, decoding, processing, and transporting data flows across terrestrial and non-terrestrial DoD platforms. In addition, solutions are sought to achieve:

RF power microelectronics component technology

A core capability of DoD 5G/6G networks is the ability to achieve RF transistor gain over a broad frequency range from 0.3-300 GHz, especially those that support dual use with potential commercial operations or provide DoD unique capabilities. For military applications, communicating between ground, air and space-based assets requires high RF power and high-linearity over broadband. At mmW frequencies, unique challenges such as increased power density and reduced gain lead to inefficient operation. Prototype demonstrations of RF microelectronics should focus on achieving high gain solutions and survivability in extreme conditions such as high-temperature and radiation environments. Compound semiconductors, ranging from narrow to ultra-wide bandgap, offer electrical properties possessing many of these niche DoD requirements.

Efficient RF integrated circuits

Demonstrated lab-to-fab RF microelectronics solutions at the circuit level can be implemented to overcome lower power transistor efficiency at mmW frequencies. For example, integrated RF microelectronic circuits utilizing harmonic tuning, load modulated balance, envelope tracking, and other waveform engineering solutions are of interest to increase chip-level efficiency for DoD platforms as is autonomous frequency agility/tunability or full-duplex operation in spectrally challenged environments.

Hybrid Microelectronic and Photonic Integrated Circuits

To meet the demands of future 5G/6G applications as well as other microelectronics initiatives such as data transport and data intensive imaging applications, enhancements in hybrid microelectronic and Photonic Integrated Circuits (PICs) are required. Innovations in interconnect technology between chiplets, FPA/ROIC bonding, optical components, and monolithic microwave integrated circuits enables integration

of ME within system SWaP constraints, as well as facilitates agility to meet mission requirements. Novel advances will also ensure hybrid circuits will be able to survive harsh environments typical of DoD platforms.

Emerging platforms for secure point-of-use DoD data networks

In order to meet future 5G/6G demands, chip I/O bandwidth must be enhanced, specifically in two areas: (1) internal computational and processing efficiency, and (2) external data transfer from one site, or High-Power Computing (HPC) unit, to another. Specifically, node-to-node bandwidth is a major driver in recovering computational efficiency. Novel chip development and system integration of co-packaged optical I/O is required to realize this bandwidth. Some examples include, but are not limited to, mmW direct conversion RF front ends, as well as technologies for accessing alternate spectrum and providing anti-tamper mechanisms including RF-photonic circuits, photonics components as well as devices that can leverage optical polarization. Similarly, high-speed networking capability will result in additional technical challenges to bring 5G/6G system level performance down to package scale, affordable at DoD levels. Hardware solutions must include AI capable designs that leverage advancements in RF signal processing, large scale digital data processing, and intelligent decision-making at the radio and network level.

C. Artificial Intelligence (AI) Hardware (HW)

The desired end-state is a fab prototype for eventual deployment in AI-enabled systems for edge applications to enable overmatch performance in operational situation awareness and decision-making in a wide variety of missions. Facilitation of the lab-to-fab prototyping and testing of these AI hardware platforms are needed.

The exponential growth of data demands advanced data analysis capabilities with higher processing performance, lower energy dissipation, and better system scalability. There is a significant gap between current AI computing capabilities and the vast amount of multi-domain sensor and operational data for high-throughput, low-latency and energy-efficient training and executing (inference) of AI models for data analytics, sensor exploitation and fusion, decision support, autonomy, etc., particularly for systems at the tactical edge where there are strict SWaP constraints and a contested network. Furthermore, the current state of main-stream AI models and their underlying computing architectures do not enable rapid adaptation to change in the actual sensor/operational data and environments, leading to degraded real-world performance such as intolerance to subtle changes in inputs (i.e., brittle) and difficulties in transitioning to a new task or environment (i.e., inflexible). Existing AI solutions also lack the appropriate computing architecture/hardware, and subsequently, algorithmic innovations to timely search decision space under complex situations and constraints, generate optimized course-of-action recommendations, and interact-learn-assist the human in decision-making.

Few commercial off-the-shelf hardware options exist today for AI edge applications. Most reduce the time required to train large deep neural networks. These current hardware options fall into two categories. The first involves specialized hardware designs (e.g., Google TPU, Qualcomm NPU) that implement optimized operations for training. The second use neuroscience-inspired designs. For example, neuromorphic chips (e.g., IBM TrueNorth, Intel's Loihi series) have performed effectively for applications involving mobile robotics, small maritime platforms, and space systems. However, they are not widely available because (1) a strong motivating (commercial) application need has not yet arisen, and (2) further study is needed to increase their performance. Additionally, nascent new materials/devices are not yet available at scale in more than R&D type foundries. Advances in the following guidance will also require validation of specified metrics.

Current industry advances were designed to capture a large consumer base. While they offer flexibility, it often results in lower efficiency and limited ability to tailor the processors to specific applications, architectures, and interfaces. Hubs should facilitate the lab-to-fab prototyping of multiple emerging AI accelerators. The following advances are needed:

Novel Neuromorphic Computing Architectures Utilizing Emerging Technologies for Extreme Edge Applications

Novel emerging memory technologies can enable energy-efficient implementation of large neuromorphic computing systems. Though large-scale learning systems have not been implemented using these devices yet, existing literature is available that discusses the ideal specifications and metrics to be satisfied by these devices based on theoretical estimations and simulations. There are emerging trends and challenges in the path towards successful implementations of large learning systems that could be ubiquitously deployed by DoD for a wide variety of cognitive computing tasks. To unleash the true potential of this hardware, advances in novel nanoelectronics, nanophotonic materials, memristor architectures, and fabrication processes are required to allow the development of platforms that realize the full potential of brain-inspired neuromorphic computing. A full end-to-end, co-designed, high-productivity software ecosystem is required for maximizing hardware system performance and efficiency. Energy-efficient AI domain-specific processors cannot operate without the support of full toolchains.

- **Edge Applications in Extreme Radiation and Temperature Environments**

Extending the efficient AI computational capability in extreme environments is needed to

counterbalance pre-existing technology being inefficient which could expose vulnerabilities. The direct exposure of AI computing devices to harsh operational environments makes the devices susceptible to high-temperature, radiation, as well as the corrosive and erosive effects of these environments. These challenging environments can limit the practical applications of those devices. Specialized AI hardware and software solutions are required to ensure reliability and durability in extreme environments. Due to the manufacturing materials, processes, and design methods, CMOS-only AI hardware may not achieve highly reliable functionality and performance in extreme environments such as high temperature and space/strategic radiations.

- **Embedded Processing for Imaging Applications**

Innovative prototype demonstrations of novel embedded microelectronics solutions are needed for high performance imaging applications. The inclusion of processing intensive tasks (AI integration, Aided Target Recognition (AiTR), image fusion, hardware acceleration, etc.) with large format, high dynamic range, high frame rate imaging systems has resulted in a data bottleneck for DOD imaging applications. Few commercial solutions exist in this space due to the specialized nature of both DOD imaging hardware and the associated image processing algorithms. New solutions are needed for low-power, embedded processing for imaging sensors. This includes advances in low-latency Readout Integrated Circuits (ROICs), Application Specific Integrated Circuits (ASICs), Photonic Integrated Circuits (PICs), wafer-to-wafer bonding/hybridization, and the associated high-bandwidth image data transportation.

- **Long Flying UAVs and Autonomous Ad Hoc Networking**

An ad hoc communications network of a group of Unmanned Aerial Vehicles (UAVs), or drones, is called a Flying Ad hoc Network (FANETs) of UAVs. Studies have shown the importance of FANETs by investigating the integration of FANETs of UAVs with different technologies, including Virtual Reality, flying edge computing, flying fog computing, cellular networks, and flying cloud computing. Although such integration brings many advantages, many issues may arise as well. The DoD is interested in capitalizing on emerging technologies integrated with FANETs and the possibilities they can open for future military extreme edge or disruptive applications.

High Performance, Energy Efficient, Reconfigurable, and Scalable Hardware

Innovative prototype demonstrations of novel computing architectures with hardware instantiations that achieve unprecedented computational performance and energy efficiency are needed. Reconfigurable hardware to address emerging requirements and simple integration with existing platforms for a wide array of operational environments are also needed. Finally, new AI-optimized hardware to address low- power Systems-on-Chip (SoC) to high-performance server implementations is also needed. Evaluation of AI hardware performance, efficiency, throughput, affordability, and SWaP under real load conditions.

Emerging AI Processing Hardware

Innovative prototype demonstrations of hardware for AI inference, adaptive AI learning, and AI optimization are needed. In addition to achieving high computational performance and energy efficiency and allowing simple integration into existing platforms, AI inference hardware that allows implementation of a broad variety of AI applications is needed. The capability to enable rapid and adaptive AI learning from new, unstructured stimuli is also needed. Finally, AI optimization hardware should timely solve some of the most challenging problems for traditional processors (CPUs/GPUs) to support an array of course-of-action applications.

Neuroscience-Inspired Designs

Computing performance advances from future complementary metal-oxide-semiconductor (CMOS)

technologies will likely be limited due to the end of Moore's Law. In addition, intrinsic limitations of the Von Neumann computing architecture, a.k.a. the "memory wall", are prohibiting AI computing platforms from meeting future data-to-decision and autonomy requirements. These limitations have motivated emerging research areas in neuromorphic computing that is inspired by the architecture and working mechanism of the human brain. At least four technology challenges must be addressed before neuromorphic chips can be fully utilized. First, current architectures include only a small number of "neurons," preventing them from satisfying the needs of computationally intensive AI edge applications. Second, these chips must operate in real-time, much like cell phones and autonomous vehicles. Third, neuromorphic chips have a SWaP advantage versus those based on the von Neumann architecture but must be scaled in complexity while satisfying size, weight, and power constraints. Finally, novel, in-situ characterization methods will be required. The ability to deliver prototypes of novel chip designs for supporting AI-enabled edge applications will require the following advances:

Neural Network Architectures

Neural network computing schemes utilize many-to-many connectivity to achieve computational tasks that evade conventional digital computing. However, a physical interconnection architecture to match that of biological neural networks has not been devised for novel nanoelectronics-based neuromorphic devices. The conventional interconnect method of defining lithographically patterned metallic lines in two-dimensional planes is unable to generate many connections beyond a few nearest and next-nearest neighbors. Additional connections require additional lithography steps, at linearly increasing fabrication cost and with diminishing returns in terms of actual connectivity increase. Crossbar structures, while enabling many-to-many connections, suffer from crosstalk between adjacent lines and are constrained to relatively few "neurons" compared to biological neural networks. The address- event representation (AER) protocol used in silicon-based neuromorphic chips, a time-multiplexing scheme, is capable of flexibly enabling massive neuro-synaptic interconnections but requires a digital interface and data exchange with remote memory, retaining the inefficiencies of the von Neumann computing paradigm. Both crossbar and AER architectures fail to replicate the variety of spike arrival timing information that arises from the length and impedance differentials of biological dendrites. The lack of an architecture to achieve many diverse and unique physical interconnections is a critical factor preventing novel beyond-CMOS neuromorphic computing devices from reaching their full potential as enablers for complex cognitive systems. The development and fab prototyping of such an architecture is imperative to fully realizing the advantages to be gained from nanoelectronics-based neuromorphic hardware.

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Reconfigurable Application Specific Integrated Circuit (ASIC) Designs

Application Specific Integrated Circuits (ASICs) have distinct power usage and processing speed advantages over reprogrammable solutions such as Field Programmable Gate Arrays (FPGAs) and Graphical Processor Units (GPUs). However, there is a large financial barrier to entry for many ASIC solutions. In addition, the design time for an ASIC can be quite lengthy. Often two or three spins are necessary to fully optimize an ASIC and thereby realize the associated technical advantages of an ASIC. Therefore, AI Hardware will

support development of a streamlined, flexible ASIC process flow or development cycle that will reduce barrier-to-entry for ASIC procurement. This new flow will focus on maximizing the amount of modularization, reuse, and reconfiguration possible within a class of ASIC design. The goal of this is to significantly reduce both ASIC design time and financial barriers for ASIC inclusion.

Neurosynaptic Devices and Circuits for High-Endurance, Uniformity, and Repeatability

Memristor-based synaptic devices for weight storage and updates in AI accelerators are expected to experience huge numbers of update cycles during training (write) as well as inference (read) cycles. They are also required to attain and hold precise and repeatable analog values that have symmetric responses to excitatory and inhibitory training events. The device characteristics must be uniform across a substrate and between manufacturing runs. Materials, devices, and circuits that are stable, uniform, and repeatable, as well as the fabrication processes to realize them, are required for the successful adoption of memristor devices into AI accelerators. Test capabilities must be available to evaluate AI hardware performance, efficiency, throughput, affordability, and SWaP under real load conditions.

Neuromorphic Devices and Architectures for Few-Shot Learning Algorithms

The device requirements discussed above (high endurance, uniformity, and repeatability) are relevant primarily with respect to conventional AI acceleration schemes utilizing deep learning neural networks. An alternative neuromorphic learning methodology to enable few-shot learning, through the organization of neuromorphic devices and circuits into novel architectures featuring massive parallelism and redundancy, would circumvent these constraints. In such an architecture, each training cycle engages a massive number of synapses sparsely distributed across a complex network of pathways, reducing the number of training cycles required for learning a given task and decreasing the cycling load per synapse device. Redundancy in the network reduces the effects of errors and non-uniformities. The new architecture, which must circumvent the Von Neumann bottleneck between processor and memory, must also expand the signaling bandwidth and fan-out between neurosynaptic devices (nodes) associated with AI learning, inference, and control.

Input/Output (I/O) Optimized for AI Processing

Data processed by AI HW comes in many forms: digital, optical/audio/haptic/electromagnetic sensor inputs, recombined memory impressions, et cetera. It is critical to convert this data into a form that is accessible to processing by the AI HW. Conversion methods include Analog to Digital Conversion, Digital to Analog Conversion, and serial-to-parallel demultiplexing and vice versa. I/O bandwidth is critical and must not become a bottleneck to the AI performance.

D. Quantum Technology

The desired end-state is a rapid-response quantum enterprise enabled by commercial foundry-like access with fast turn-around times. Access to these fabrication facilities, which are amenable to developing process design kits (PDKs) for a variety of leading qubit platforms and support technologies, should be provided to DoD, DoD supported university/academic based collaborators as well as support the U.S. commercial quantum technology industry needs.

Subsequently, fast tape-out schedules for academics and industry will both enhance the feedback time for established researchers and open the possibility for new groups or companies to better explore the landscape of qubit chip designs which may be viable for transitions to large scale implementations. The goal is to assist in the development of quantum processor quality and capability as well as quantum sensor and quantum networking. To achieve this end-state, multiple needs must be addressed including test, measurements, assembly, and packaging.

Integration

Quantum technology requires specialized Systems on Chip (SoCs) that are capable of preparing, manipulating, and measuring quantum information as well as operating classical control algorithms to utilize that quantum information, all at the required fidelity and speed for technological advantage. Hubs will need to facilitate the advancement of multiple emerging microchip platforms, integration of those platforms, and novel test and measurement capability. Specialized quantum packaging and assembly will be needed including tool optimization and integration that requires environmental considerations (e.g., cryogenic cycling for superconducting qubits).

There are several quantum platforms (QP) technologies being developed in the U.S. private sector that promise to scale to advantageous computational size including, but not limited to, superconducting quantum bits (qubits), semiconductor spins, ions, neutral atoms, solid state color centers and photons, each of which have several variations. These diverse technologies may have varying needs so it is not necessarily expected that one solution will be able to support all possible quantum technologies; however, it is expected that solutions support the multiple needs of the QP technologies proposed.

Quantum Technology hubs are not meant to support the direct "scaling up" of quantum computing technologies to compute size of economic advantage. This is a matter for quantum computing companies to address using advancements made within the MEC Quantum Technology hubs. The hubs are meant to accelerate the capabilities of the micro fabricated quantum chips and SoCs and related quantum technology areas to advance more quickly. Therefore, at this time, Government funding from Commons will not be applied to quantum computing chips projects with more than 200 physical qubits. This constraint may change in the future as quantum computing power increases. Innovative solutions are requested to achieve the following advances:

Emerging Platforms and Materials

Quantum technology is built on a collection of emerging micro fabricated platforms including superconducting platforms, large band-gap photonics, non-linear optical materials, and other specialized materials. The acceleration of research in some of the leading qubit types is still hampered by lack of reliable access to these high-quality materials. Examples include clean superconducting materials with high surface quality, isotopically purified silicon-28, materials with high second and third order nonlinear coefficients, and materials like diamond or SiC that can host defect color centers. Some qubits also required engineered hybrid superconducting/semiconducting materials such as hybridized systems to support next-generation single- and entangled-photon states. Establishing formal channels by on shoring to secure supply chain and/or processes for acquiring these materials will speed up research progress.

These quantum platforms can have fabrication and packaging requirements that differ from other microelectronics. For example, large temperature cycling between fabrication, often at high temperature to improve surface roughness, and operation often at cryogenic temperatures. The temperature range presents a significant challenge. The emerging quantum ecosystem requires advances in these emerging platforms to realize the potential of quantum technology. For trapped-ion and neutral atom platforms that present valuable computing as well as RF inertial and magnetic sensing applications, enabling technologies for integration can serve as drivers such as on-chip trapping electrodes and waveguide-to-free-space optical coupling using diffractive or meta-optics. In solid-state quantum platforms, integration of an ASIC with any proven solid state quantum system, such as SiC or diamond NV with on shore sustainable sources for the entire supply chain (seed to circuit) are highly desirable.

Packaging will include challenges such as low-loss electronic/photonic packaging for advanced quantum systems, including cryogenic electronic-photonic integration (down to the milliKelvin), heterogeneous integration of qubit technologies, materials, and methods to scale at the 200/300 mm wafers, new electro/optical materials integration such as on-shoring thin film Lithium Niobate (TFLN) and barium titanate insulator wafers to advance these quantum platforms and technologies.

Achieving the stringent requirements for quantum systems benefit the entire community with many of the platforms being dual use for other technology areas of interests to DoD and commercial sectors. High-performance nonlinear optical materials, including thin-film lithium niobate or barium titanate-on-insulator which is suitable for a variety of RF photonics and surface-acoustic-wave devices. SiC-on-insulator can be used for quantum photonics as well as high-power, high-temperature electronics – methods to on-shore and scale these technologies will be valuable for a variety of use-cases.

Quantum Support Chips and Integration

These specialized QPs are not thought to operate alone but will need support from “classical” microchips that are themselves specialized. QPs, depending somewhat on the type of qubits onboard, need integrated transistor logic, specialized amplifiers, modulators, and filters, monolithic microwave integrated circuits (MMIC), and photonic integrated circuits (PIC) operating at shorter wavelengths – all of which require low electrical- and optical-loss. These Quantum Systems of Chips (Q-SoCs) will require advances in these support chips as well as three-dimensional integration and packaging techniques. The integration will be all the more difficult because the qubits on QPs are typically fragile and susceptible to stray electromagnetic fields. Specific examples include developing multilayer, microwave-integrated, three-dimensional microwave heterostructures for superconducting qubits, integration of cryogenic CMOS with qubits, and integration of PICs with high bandwidth and high extinction to address atomic systems or color centers. Q-SoCs will require on-chip narrow-linewidth mode hop-free tunable and stabilized sources at visible to near-IR wavelengths and on-chip, high-efficiency light collection and detection. Quantum sensors, of many types need access to integrated photonics components and, separately, superconducting materials that may be distinct from qubits for computing.

Demonstrations of quantum platform advances to enable inertial sensors/ atomic gyroscopes based on either trapped ion, vacancies, Rydberg atoms, or optical combs is an important aspect.

Test and Measurement Capability

QPs are difficult to characterize because they operate in a regime where quantum effects become apparent (for example in vacuum or at low temperature) and those quantum effects may present unique observation challenges. Exquisite control and isolation from external noise or disturbance that can cause decoherence or alter quantum state, high-sensitivity camera for accurate monitoring, and measuring heat flow through nanoscale devices all pose challenges in test and measurement to name a few. Next generation and scalable single photon sensing and entangled photon generation/sensing with high

fidelity are critical.

Specialized quantum packaging and assembly for integrated quantum chips must be addressed for PICs and SC platforms to enable commercialization and system applications. Unique shielding, heat dissipation, long-term hermeticity, vapor-cell integration, are some examples of challenges to overcome.

Other Desired Outcomes

It is desired that access to non-quantum-based electronics experts outside of quantum physics. Additional desired outcomes of Quantum Technology hubs include, but are not limited to, the following demonstrations: 1) cryogenic quantum systems with classical electronics; 2) photonic integrated circuits with gain, low-loss, and non-linear device sections on one platform; and address challenges such as scalable integration of on-chip light sources including single/ entangled photon sources, and the importance of methods to increase the rate and fidelity of single and entangled photon generation. The detection of single- and entangled- photon states, including the use of number-resolving detectors a low-loss active waveguiding material for short-wavelengths/ wide-bandgaps 3) integrated single photon detectors and high-flux, high-fidelity entangled photon sources. Demonstrations of SWaP or performance improvements such as through integration with classical or quantum photonic/ electronic integrated circuits, with repeatable processes and methodologies should be a part of the solutions.

E. Electromagnetic Warfare

The future of Electromagnetic Warfare (EW) reflects a paradigm shift from the traditional approach of deploying disparate systems to perform singular functions within a rigid spectrum allocation. Modern EW (Radar, Electronic Support Measurers, Electronic Attack, and Electronic Protection) requires rapid deployment of capabilities to outpace the threat using force-level, multi-function systems with ability to sense presence of targets and threats using all the Electromagnetic Spectrum (EMS). While the multi-function systems approach is increasingly more synergistic, there remain many situations where EW specific systems and corresponding microelectronic components are more appropriate to reduce cost and complexity. Both multifunction and specific system approaches are appropriate within the MEC framework.

The desired end-state is lab-to-fab maturation of prototypes to support EW, as well as other EMS activities, existing primarily in the application space consuming digitized data from multi-platform sensors and transmitting via programmable multi-function apertures. Hubs will facilitate lab-to-fab maturation of critical microelectronic technologies and applications for transmit, receive, digitization, transport, and processing of received EMS signals for EW missions. Many EW systems rely on Active Electronically Scanned Arrays (AESA) where a basic module is used as the building block. The module should be highly integrated, scalable, multi-function, easily reconfigurable, robust, and have low SWAP+C.

Those EM and EMS activities described above are enabled by Domain-Specific Systems-on-Chip (DSSoCs) and discrete chips providing electronic survivability, electronic attack, and electronic support at a wider range of operating frequencies, instantaneous bandwidths, and resolution/bit-depth. All of this must be accomplished with improved form factor and thermal efficiency for DoD to gain technological advantage.

There are several EW relevant chip ideas being developed in the commercial sector including, but not limited to, high frequency RF digital to analog converters (DACs/ADCs), RF systems on chip (RFSoCs), digital readout integrated circuits (DROICs), AI-accelerating hardware, high-speed networking, ultra- wide bandgap semiconductors for both RF and power, and simultaneous transmit and receive (STAR) that can bring EW system-level performance down to package scale.

While the commercial sector technologies show relevance, additional lab-to-fab maturation efforts of ME and support electronics are required to ensure that technology satisfies stringent military requirements. In addition, military devices often operate at higher power and higher temperatures as compared to those used in the commercial sector. Improvements are required for domestic foundries to support existing high temperature materials and increase the transistor per chip area capability. Lab-to-fab prototype demonstrations to achieve the following advances are needed:

Emerging Platforms

EW technology and especially EW edge (edge defined as literally at an edge of a sensor system, or the most forward platform in combat operations) computing technology is currently built predominantly on commercially available field programmable gate arrays (FPGAs), precluding a fundamental technology advantage for the U.S. In addition, these components and sub-systems can have tight form factor requirements that differ from other microelectronics such as conformality, higher temperature, shock, and vibration.

Platform signal and data processing must rapidly and efficiently combine all sources of information into a coherent and manageable interface for both weapon systems and human operators. The ability to rapidly apply Artificial Intelligence/Machine Learning (AI/ML) algorithms across the broad expanses of the Electromagnetic (EM) environment will be essential for removing the ambiguities of the complexity expected in future environments. AI/ML chips will be needed to assist weapon systems and human operators manage the volume of information being received. An automated means to make sense of data streams and to remove clearly redundant information will be required.

Directed Energy (DE) Electronics

The DoD requires advanced microelectronics for non-kinetic directed energy weapons. Lab-to-fab solutions such as those producing state-of-the-art electrical performances in high-voltage fast-opening switches, beam control, microwave and mmW RF microelectronics, pulsed power of electromagnetic energy, and others for DE applications.

Support Electronics

Application specific EW chips do not operate independently from support electronics such as filters, power, control, status, and calibration/timing devices, which are specialized and serve as primary contributors to EMS sensor SWaP. Onboard logic, RF, and power electronics will vary at both the chip and package level as a function of architecture and platform constraints. Systems-in- Package (EW-SiPs) will require lab-to-fab maturation of these support electronics.

Examples of support electronics and their impact on performance include 1) compact tunable high-performance filters to enable high performance across the EMS, 2) innovations in DC-to-DC converters enable increased power densities with improvements to efficiencies, and 3) built-in measurement, built-in test, and calibration electronics enabling confidence in system mission readiness and optimized performance.

Adaptive Filter Technologies for Wide-Bandwidth Direct Digital Actively Electronically Scanned Array (AESA)

The EW ecosystem of the future will increasingly feature multi-band, digital-at-every-element architectures that allow AESAs to perform beamforming in the digital domain which enable the collection of many beams simultaneously. Any resultant agile filter solution should seamlessly support multi-band operations to provide RF front-end EMI protection and DAC/ADC noise and spur rejection within element spacing constraints.

Wideband High-Power Radio Frequency (RF) Device Technology Operating in the Millimeter-Wave Spectrum

The DoD will benefit from innovative microelectronic technologies that spur the growth of high-power RF devices which provide measurable improvements in efficiency and operational bandwidth. Desired millimeter-wave regime devices will demonstrate increased power density, reduced size, excellent gain, and improved reliability.

Radio Frequency (RF) Optoelectronic Technologies for Wide-Band Direct Digital Actively Electronically Scanned Array (AESA)

The DoD will benefit from advances in optical synthesizers and optical processing devices to improve size reduction and increased performance. The emphasis should be in providing heterogeneous integration of optoelectronics, RF, control, and power devices providing wideband RF to optical conversion early in the RF sensor receive chain. End-state technologies will demonstrate a mix of innovative timing, filtering, beam steering, processing, Electromagnetic Interference (EMI) suppression, and Digital to Analog Conversion (DAC)/Analog to Digital Conversion (ADC) capabilities in the optical domain.

F. Commercial Leap Ahead Technologies Lab-to-Fab Maturation Areas of Interest

Commercial Leap Ahead Technologies develops revolutionary capabilities that are nearing prototyping and early commercialization that must be refined and quickly given to the warfighter[1].

Lab-to-fab maturation may include but are not limited to:

High-Power Wide Bandgap RF Ecosystem
Lab-to-Fab maturation of Wide Bandgap RF devices. An area of interest is Lab-to Fab maturation for advances in device level thermal management for III-nitride RF devices. Candidate approaches to enhance thermal management are integration of diamond films, elimination of GaN/SiC interface with poor thermal boundary resistance, diamond-all-around, buffer-free III-nitride RF device with elimination of GaN/SiC interface, 200mm diameter wafer-level temporary bonding and release of the GaN device layer separated from GaN Engineered Substrates, optimized thermal material interface to the GaN device layer separated from thinned GaN Engineered Substrates, and other advanced thermal management approaches. GaN HEMT RF power densities above 40W/mm at X-band using a scalable process is desired.

Electronics for Extreme Environments (Radiation, Temperatures) Including for Space and Hypersonics

Lab-to-Fab maturation is desired for high temperature and radiation hard RF, analog, digital, and memory technologies for future applications to avionics, hypersonic systems, geothermal, and space systems. An area of interest is high temperature silicon-on-insulator (SOI) technology for analog, logic, and memory. The high temperature SOI should operate reliably from -50 to 350 °C ambient temperature and have the capability for excursions to 400 °C ambient temperatures. High temperature SOI SRAM is also of interest.

Electro-Optic Materials

- *For Photonic Integrated Circuits*: Electro-optic materials (and more generally nonlinear optical materials) have cemented their place with the integrated photonics toolbox as a platform that can bring amplitude- and phase-modulators, optical isolators, and wavelength converters for applications such as electronic warfare, optical communications, active sensing, and quantum information. Materials such as single-crystal lithium niobate on insulator (LNOI a.k.a. thin-film lithium niobate, or TFLN), barium titanate on insulator (BTO-OI), have proven the capability to extend to 150mm wafers at reasonable yields. On-shoring this capability and instantiating a wafer-scale foundry-level process to produce components for selected wavelengths will provide a pivot for aforementioned DoD technologies, as well as numerous commercial photonics applications such as autonomous automobile navigation, advanced sensing in consumer electronics. Areas of interest include 1) Lab-to-Fab development for high quality 150 mm diameter TFLN on 2-micron thick silicon oxide on silicon wafers, 2) Lab-to-Fab for die-to-wafer bonded TFLN on silicon oxide on 200 mm wafers, and 3) Lab-to-fab development for optimized TFLN-OI and BTO-OI integrated photonic technology. Successful processing would provide PDKs, and ideally MPW runs for low-loss, high-frequency, high-performance components, periodically-poled solutions for phase-matching in frequency converters.
- The desired end-state(s) are prototypes that lead to the adoption and integration of revolutionary, capability-enabling (i) material platforms and their manufacturing, (ii) methods for power delivery and dissipation, and (iii) operational modalities that leap ahead of existing commercial optoelectronic products at higher performance and/or efficiency. Hubs will facilitate developments into micro-electronic and micro-optoelectronic devices comprised of revolutionary materials and advanced power management solutions that go beyond established solutions available in the commercial sector in one or more performance metrics.

Advancement in Magnetic Tunnel Junction Technology for Advanced Memory

Lab-to-fab maturation are desired for improvements in the density, high temperature characteristic, and/or radiation hardness of magnetic tunnel junction technology for DOD applications. Capabilities of interest include scaling memory technology below 20 nm feature size and have a write error rate (WER) below 10^{-7} at 125 °C or 150 °C. While spin-transfer torque (STT) and spin-orbit torque (SOT) are commercially available, new lower technology readiness level (TRL) concepts for MRAM technology are being developed such as voltage-controlled magnetic anisotropy (VCMA), voltage-gate assisted spin-orbit torque (VG-SOT), domain technology devices, multi-layer magnetic tunnel junction (MTJ) devices, and other concepts. A goal is to transition advanced MTJ devices that are ready for lab-to-fab transition. The MRAM cells should have standby stability at relevant operating temperature and radiation dose.

Acoustic Wave Filters
Lab-to-Fab maturation is desired for Bulk Acoustic Wave (BAW) Filters. An area of interests is high-power, high linearity, high Q solid mounted resonator (SMR) BAW with an acoustic reflector implemented in the substrate with optimized temperature coefficient frequency (TCF) layer and optimized bottom and top electrodes for enhancing Q. Optimization of the temperature coefficient frequency layer is needed to not degrade the power handling. Methods to reduce spurious modes using frame structures and phononic structures should be implemented. Additional designs may use a SMR-XBAR configuration. Optimized thermal conductivity is needed for high power capability. The trade-offs of optimizing different characteristics the acoustic wave filter should be made for an appropriate DoD application(s).

SOI and Wafer Bonding of Enhanced 3D devices/Integrated Circuits
Lab-to-Fab maturation is desired for silicon-on-insulator (SOI) and enhanced 3D integrated circuits.

An area of interest is non-liquid approaches to enable DRAM memory on logic processors. The roadmap for the commercial industry is to implement High Bandwidth Memory (HBM) on logic processors/memory controllers in 2026 and implement HBM on high performance logic processors for artificial intelligence and high-performance computing in 2028. In addition, implementing DRAM on logic processors can enable new processor architectures such as compute in memory. The DRAM temperature must be below 80C to have adequate refresh time. Non-liquid cooling approach are desirable for compact implementations while liquid approaches are needed for integration of DRAM with high performance processors. The topic of interest is to optimize the approach for the non-liquid cooling approach. The non-liquid cooling approach requires three areas of optimization: 1) a laterally thermally conductive material layer that would transfer heat to copper filled through silicon vias (thermal vias), 2) a thermal isolation layer, and 3) EDA design that would optimize the 3-dimensional location of the DRAM to not be stacked over hot spots in the logic process. The goal of this topic is to optimize the laterally thermally conductive material layer and the thermal isolation approach that could be transferred in the future to an advanced CMOS foundry. It is not the intention to support the development of a logic processor with the laterally thermal conductive material layer and the thermal isolation approach. Test chips can be fabricated with the optimize lateral thermal conductivity layer and thermal isolation approach. Papers in the literature have proposed aluminum nitride as the laterally thermal conductive layer. An investigation could be conducted to optimize the aluminum nitride material layer or investigate other material layers. Other approaches to investigate laterally thermal conductive layers and thermal isolation approaches are appropriate. It is not the intention of this topic to support liquid immersion cooling, interposers with liquid cooling, two-phase cooling, or other liquid based cooling.

Wafer bonding has many applications to integrated photonics, single-crystal semiconductor engineered substrates, and numerous additional applications. Wafer bonding can be applied to many of the topics of this call for all technology areas.

Lab-to-Fab maturation is desired for advances in SOI and wafer bonding. An area of interest is SOI wafer manufacturing in a trusted environment. Develop a trusted manufacturing flow for production-level manufacture and processing of radiation-hardened ultra-thin body and box (UTBB) SOI wafers. Develop trusted flow for handling radiation-hardened wafers from manufacture to final device fabrication at a

domestic facility.

Emergent Material Platforms
Expanding the fundamental capabilities of microelectronics and packaging for sensors, computing architectures, and memory storage at reduced SWaP requires manufacturing improvements for high-yield, low-defect processing of new material systems in place of traditional semiconductor platforms. Poor quality wafer scale growth at manufacturing volume of candidate optoelectronic material alternatives, such as two-dimensional materials (e.g., molybdenum disulfide), semiconductor alloys (e.g., silicon germanium tin), and/or low dimensional crystals (e.g., quantum dots) have largely precluded realization of commercial devices that leverage their full technological potential. Other emergent material systems with potential for domestic sourcing in raw elemental, molecular, or mineral form and high-purity refinement techniques are of interest to strengthen supply chain availability for microelectronics. Domestic sourcing and synthesis of high quality, new material platforms is a fundamental precursor to innovative device designs with new degrees of freedom.

Standardization of Hybrid Optical-Electrical Signal Processing Architectures
Signal processing and computing devices built upon electronic integrated circuitry, and, more recently, PIC, are built upon standardized, analogous components (e.g., resistors vs. waveguides) that allow a common toolset for designing new products. Hybrid devices built upon open systems architecture concepts with data-fused electronic and photonic constituents can strategically leverage the strengths of each to execute signal processing tasks on-chip, including artificial intelligence and neural networks, towards actionable data to circumvent user judgement/interpretation. However, further innovations are required to standardize the design toolset of hybrid circuitry devices to balance speed, SWaP, and data fidelity. Other approaches to embedded, intelligent processing beyond the traditional serialized detector-processor-algorithm approach could provide competitive opportunities.

Power Management
Fielding of distributed, fused sensor networks in the Internet of Battlefield Things (IoBT) with practical SWaP requires innovations in power delivery concepts and embedded thermal management schemes. Prototyping opportunities exist for integrating solid-state energy harvesting concepts for sustained operations. Existing thermal management approaches to electrical processing devices, especially in nanometer-scale node technologies, govern their performance (e.g., clock speed) and SWaP. New materials, devices, and architectures can be demonstrated via packaging schemes that incorporate innovative heat rejection and dissipation concepts to circumvent traditional SWaP penalties of adding conductive thermal mass and/or convective heat exchangers.